REMARKS

Claims 1-3, 5-11, 13-22, 24-42, all the claims pending in the application, stand rejected on prior art grounds and upon informalities. Claims 5-6, 13, 25, and 34 stand objected to. Applicants respectfully traverse these rejections based on the following discussion.

I. Objections To The Claims

Claims 5, 6 and 13 are amended herein to correct typographical error and/or to reflect dependence from a non-cancelled claim.

As claim 25 was clearly amended in the 27 March 2007 response, it is now listed as previously presented and present in a clean (as opposed to marked-up) form.

As claim 34 was clearly not amended in the 27 March 2007 response, it is now listed as previously presented.

II. The 35 U.S.C. §112, First Paragraph, Rejection

Claims 1-3, 5-11, 13-22 and 24-42 stand rejected under 35 U.S.C. §112, first paragraph, as based on a disclosure which is not enabling. Specifically, the Office Action indicates that "Claims disclose generating computer model based on a target model where the target model is created using the performance parameters –the disclosure lacks enablement for creating such a computer model effectively based on performance parameters, which is critical or essential to the practice of the invention, but included in the claim(s) is not enabled by the disclosure." These rejections are traversed as explained below.

The Applicants respectfully disagree with the assertion that the disclosure lacks enablement for creating such a computer model effectively based on performance parameters.

Paragraph [0023] acknowledges that different teams are involved in the design/manufacture of a final product. A device designer creates individual devices and the circuit designer utilizes the different devices to create a complete integrated circuit. However, problems can occur as device design progresses (see paragraph [0025]), which in turn can present a potential problem to circuit designers (see paragraph [0026]). Thus, the invention creates "a target model of the device" using target performance parameters for the device and device goals (see item 406 of Figure 4 and paragraph [0034]). "The circuit design process relies upon the target performance parameters 404 and target model 406 to create a circuit model 434 of the chip" (i.e., to create a computer model of the integrated circuit). This circuit model is then simulated in item 436 and the results of the simulation are checked to determine whether the circuit goals have been met (438) (see paragraph [0035]). Paragraph [0038] provides that this "inventive target-based compact model allows designers to evaluate variations in the process while maintaining the performance targets set out by the target model." Consequently, the Applicants submit that process of generating a computer model for an integrated circuit based on a target model for a device where the target model is created using the performance parameters is enabled by the disclosure.

Furthermore, claims 1-3, 5-11, 13-22 and 24-42 are all the claims presently pending. Claims 1, 9, 14, 19, 24, 36, 40 and 42 are each independent claim. However, only independent claims 1, 9, 24, 40, and 42 reference "a computer model". Claims 14, 19 and 36 are not limited by "a computer model". Therefore, since independent claims 14, 19 and 36 (as well as their respective dependent claims 15-18, 20-22 and 37-39) do not claim "a computer model", a rejection as to enablement of such a computer model is not warranted.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. The 35 U.S.C. §112, Second Paragraph, Rejection

Claims 1-3, 5-11, 13-22 and 24-42 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding independent claims 1, 9, 14, 19, 24, 36 and 40, the Office Action provides that the claims disclose "limitation "first bound range" and "second bound range" for a "performance parameter". However, no specific ranges are provided by this claim thereby failing to provide for the metes and bound for the ranges." These rejections are traversed as explained below.

Claims 1, 9, 14, 19, 24, 36, 40 and 42 includes the features of "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range"; "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point"; and "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device." While no specific ranges are provided in the claims, none are required. The range is application specific, as claimed. That is, each first bounded range is a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of the model curves for different designs for the device that achieve a same

performance point. Similarly, the second range is constrained by at least two of these curves so as to comprise performance parameter variations between multiple different designs for the device.

Support for these ranges is found in paragraphs [0020]-[0030] of the published patent application and Figures 2-3. Paragraph [0020] indicates that rather than specifying the performance parameter as a single target point, the parameter is expressed in terms of its permitted variability within a range constrained by at least two variables (i.e., within a target performance parameter range). The first variable being the manufacturing process and the second being variations in device design. Paragraph [0025] further explains that variations in a design of a device (that achieve the same performance point may results in different model curves (see curves 20-22 of Figure 2 representing multiple different designs for the same device). That is, curves 20-22 were based on the same target model. Thus, as explained in paragraph [0028] the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., it includes the second bounded range as claimed). Paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on processes windows (i.e., first bounded ranges, designated by dashed lines in Figure 2) around each of the design curves 20-22.

Specifically, as illustrated in Figures 2 and 3 and explained in paragraphs [0029]-[0030], the final target performance parameter range 30 includes all point between curves 20 and 22 (i.e., includes a second bounded range). It is further expanded to include all points between the upper edge of 27 of the processing window (i.e., the first bounded range) that is located around the most linear curve 22 and the lower edge 25 of the processing window (i.e., another first bounded

range) that is located around the least linear curve 20 of the second bounded range). Thus, the final target performance parameter range also includes multiple first bounded ranges.

Again, no specific range is provided in the claims, nor is one required because for any given device the first bounded ranges will vary due to manufacturing process variations and the multiple model curves for different designs of the device that achieve a same performance point and the second bounded range will also vary based on the multiple model curves for the different designs of the device. That is, the ranges are application specific, as claimed and as described in detail in the specification. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

IV. The Prior Art Rejections

Claims 1-27 and 30-42 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hershenson, et al., (U.S. Patent No. 6,269,277), hereinafter referred to as Hershenson, in view of Krivokapic, et al. (U.S. Patent No. 5,966,527), hereinafter referred to as Krivokapic, further in view of applicant's own admission. Claims 28-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hershenson, in view of Krivokapic, further in view of applicant's own admission, further in view of Peng et al. (U.S. Patent No. 6, 028, 994), hereinafter referred to as Peng. Applicants respectfully traverse these rejections because the cited prior art references do not teach or disclose the following claimed features of independent claims 1, 9, 14, 19, 24, 36, 40 and 42: (1) "wherein said target model is created using a target performance parameter range for said performance attribute" (and, specifically, where a computer model of an integrated circuit is generated based on this target model, where the target

model is of a device that is a component of the integrated circuit, and where the performance attribute is a performance attribute of the device); (2) "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range"; (3) "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point"; (4) "wherein each of said multiple different designs is directed to a variation of a single design for said integrated circuit"; and (5) "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device."

A. Summary Of The Cited Prior Art References.

Hershenson provides a system for providing automated synthesis of a globally optimal designs for a given circuit topology library. Specifically, referring to col. 5, line 35-col. 6, line 25, Hershenson provides that when a new semiconductor manufacturing process is initiated on the CAD system, models for the transistors (i.e., for a single component of an IC) are generated. The CAD system may include posynomial models of different levels of complexity that can be selected as needed based on the design requirements. The CAD system also includes a library of circuit topologies. Topologies are generally understood to be configurations (i.e., a relative arrangements of components, parts or elements (see Merriam-Webster Online Dictionary copyright © 2005 by Merriam-Webster, Incorporated). The library is divided into groups based on multi-component device type (e.g., op-amps, amplifiers for automatic gain control, limiters, oscillators, etc.). Thus, it is understood that the library includes, for each multi-component

device, one or more different topologies or different relative arrangements of the individual components (e.g., transistors) within the devices.

After a transistor model is selected, a user selects a circuit topology or group of circuit topologies for the device from the library and then selects performance specifications for the desired device (i.e., for the desired circuit topology, such as an op-amp, oscillator, etc.). More specifically, for a given multi-component device (e.g., an op-amp) the user determines the design parameters and performance specifications (see col. 10, line 35-col. 11, line 30). The system then generates a geometric program for the defined performance specification of the multi-component device, and based on a user-selected optimization mode, reformulates the geometric program as convex optimizations problems (see col. 7, lines 60-67). The program solves the geometric program for a globally optimal design of the integrated circuit topology for the user-defined defined specifications.

Krivokapic discloses a method for simulating the behavior of a mass-produced device. Specifically, Krivokapic recognizes that a designer must consider numerous transistor attributes in predicting semiconductor behavior and that a designer often must balance conflicting attributes to achieve a desired behavior (e.g. drain-to-source current vs. drain-to source voltage curves (I/V curve)). Various prior art device simulators model designed transistor behavior. However, prior art modeling do not accurately reflect mass-produced semiconductor device and do not use semiconductor manufacturing process simulations to generate distributions of manufactured semiconductor devices (see col. 3, line 66- col. 4, line 3). Thus, Krivokapic discloses an improved method for modeling designed transistor behavior in which I/V curves are obtained and used to show how choice of semiconductor device attributes, such as channel

length, effect the guard band or manufacturability of such devices (see col. 4, lines 26-34). Specifically, referring to Figure 5 and the related text, performance values are obtained from devices with different attributes (step 500). A device simulator is calibrated based on the performance values (step 501). A process simulator is calibrated based on the performance values and the measured attributes of the devices (step 502). The process simulator is run (step 503). Then, the results of the process simulator are input into the device simulator to obtain I/V curves (step 504) and to determine the statistical worst-case I/V curves (step 505) by averaging the drain-to-source current values associated with drain to source voltage values. Parameters for device simulators are then extracted from the statistical worst-case I/V curves (step 506). The device simulator will output worst-case I/V curves in response to input parameters obtained from the statistical worst-case I/V curves (step 507) and finally, the worst case I/V curves can be compared to an ideal curve to obtain manufacturing guard bands (step 508).

B. Summary Of The Present Invention.

Contrarily, the present invention is concerned with creating a computer model for an integrated circuit using not only circuit goals for the integrated circuit itself, but also a target model for a device that will be incorporated into the integrated circuit. The target model for the device is created using a target performance parameter range for a given performance attribute of the device. This target performance range is further constrained by two variables (the device manufacturing process and device design). Specifically, the target performance parameter range comprises multiple first bounded ranges and a second bounded range. Each first bounded range represents a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of the device

that achieve the same performance point. The second bounded range on the other hand is constrained by at least two of these multiple model curves (i.e., it comprises performance parameter variations between multiple different designs for the device.)

C. All Of The Claim Limitations Are Not Taught Or Disclosed.

The Office Action provides that both Hershenson and Krivokapic teach "wherein said target model is created using performance parameter ranges for said performance attribute (HE'277: Col. 5 Lines 40-46; Also see ranges in KR'527 Fig. 1 Elements 103-107)." The Applicants respectfully disagree. It should be noted that the claimed feature is "wherein said target model is created using a target performance parameter range for said performance attribute", not simply "wherein said target model is created using performance parameter ranges for said performance attribute."

In Hershenson, a user selects a transistor model and a circuit topology from the CAD library and defines the performance specifications for a multi-component device (i.e., a circuit, such as an op-amp) (col. 5, lines 63-68). The system of Hershenson then generates a globally optimal design solution for achieving the defined performance specifications (see col. 5, line 68-col. 6, line 25). Col. 5, lines 40-46 specifically provides that "When a new semiconductor manufacturing process is initialized on the CAD system of the present invention, models for the transistors in the process are generated. The system may include posynomial transistor models of different levels of complexity that can be selected as needed based on the design requirements." That is, the system of Hershenson may include multiple device models with different levels of complexity depending upon the design requirements. But Hershenson does not teach or disclose that a target model for a device (which is a component of an integrated

circuit) is created using a target performance parameter range for a given performance attribute of that device, much less that such a target model is subsequently used to generate a computer model of the integrated circuit.

The background of Krivokapic discusses that various device simulators have been built to model designed transistor behavior based upon specified transistor attributes (see col. 2, lines 33-38). Figure 1 of Krivokapic illustrates such a prior art method of modeling (to obtain I/V curves) (see col. 2, lines 39-42). Items 103-107 of Figure 1 refer to five specific sets of parameters required by one semiconductor device simulator (see col. 2, lines 55-59). The parameters 103-107 are extracted from a device parameter extractor and correspond to physical measurements or are derived from physical measurements of the transistor (see col. 2, lines 60-64). These five process parameters 103-107 are referred to as the five corners and illustrate the operational or behavioral envelope of typical manufactured device (col. 3, lines 32-35). Based on these measured and derived parameters, designers can model with a simulator, the worst-case IV curves and how the worst case transistors affect a circuit (see col. 3, lines 35-40). Thus, the cited portion of Krivokapic models the IV curve of a device using the overall operational/behavior envelope of a typical device (i.e., using actual measured parameters or parameters derived from measured parameters from the same type device manufactured under various different process conditions) (see col. 3, lines 5-40). It does not create a target model for a device (which is a component of an integrated circuit) using a target performance parameter range for a given performance attribute of that device, much less that this target model is subsequently used to generate a computer model of the integrated circuit.

The Office Action further provides that Hershenson "teaches *target performance parameter range comprises multiple first bounded range* (due to process variation being modeled as inequalities –HE'277-single variation as function f_o and multiple variations as f_i-Col. 7, line 1-59; Col. 20 Lines 6-21, Col. 21 Lines 10-34; specially see Col. 20 Lines 35-41" *and a second bounded range* as inequality constraints (due to variation of multiple design in complexity for a transistor (or said device)-HE'277: Col. 5 Lines 40-48. The Circuit topologies pointed out further for more complex elements e.g., (herein the product built from the device HE'277 Col. 5 Lines 50-51) are based on the selection of one of designs of the transistors ranging from simple to complex. When the topologies are optimized a design is selected based on the required performance parameters (HE'277: Col 6 Lines 21-35)." The Applicants respectfully disagree.

Specifically, the Applicants respectfully disagree with the finding that col. 7, line 1-59; col. 20, lines 6-21; col. 21, lines 10-3; and col. 20, lines 35-41, of Hershenson, teach the multiple first bounded ranges feature of the present invention. Hershenson at col. 7, lines 1-5, indicates the invention optimizes circuit design by modeling circuit operation using geometric programs and solving the geometric programs to provide optimal design parameter values. Col. 7, lines 5-59, describes generally that a geometric program is an optimization problem having a specified form without references to what variables are used in the equations or what they solved for. Col. 20, line 6-col. 21, line 67, discusses an additional embodiment of the invention where the method is for developing a circuit design that meets a set of specifications for a set of values of parameters rather than specifications for known or fixed parameters. The Applicants submit that *a set* of specifications for *a set* of values of parameters necessarily does not amount to the *multiple bounded first bounded ranges* included in the target performance parameter range of the

claimed invention. Additionally, the referred to values of parameters (e.g., transistor threshold voltages, mobilities, oxide parameters, channel modulations parameters, supply voltages, and load capacitances) correspond to specifications for a circuit and not to the specifications for a device (e.g., a transistor) that is incorporated into the circuit, as in the present invention. That is, in the present invention, the target performance parameter range is used to create a target model for a device and then a computer model for a circuit that comprises the device is generated based on the target model. Whereas, in one of the method embodiments of Hershenson, a transistor model is selected from a library and the circuit topology is also selected (see col. 5, lines 63-65). Next, a set of specifications to meet a set of values of parameters for the circuit is selected (as opposed to specifications for known or fixed parameters of the circuit) and then the geometric program is generated (see col. 20, line 6-col. 21, line 68). Thus, Hershenson does not teach or suggest that the target model for a device within an integrated circuit is created using a target performance parameter range for a performance attribute of the device, much less that this target performance parameter range of the device's performance attribute comprises "multiple first bounded ranges".

The Applicants further disagree with finding that col. 5, lines 40-51 and col. 6, lines 21-35 of Hershenson teach the second bounded range feature of the present invention As discussed above, col. 5, lines 40-48, of Hershenson provides that "When a new semiconductor manufacturing process is initialized on the CAD system of the present invention, models for the transistors in the process are generated. The system may include posynomial transistor models of different levels of complexity that can be selected as needed based on the design requirements." That is, the system of Hershenson may include multiple device models with

different levels of complexity depending upon the design requirements. Col. 5, lines 50-51 of Hershenson provides that the CAD system can include a library of circuit topologies for a large number of devices. Col. 5, line 61-col. 6, line 36 provides that after a transistor model is selected from the library, a circuit topology or group of circuit topologies can be selected and further selects the performance specifications for the desired device (i.e., for the circuit itself not the transistor). The system of Hershenson generates a geometric program by selecting one of three optimization modes. The solution provided is a globally optimal solution for the defined circuit performance specifications. Thus, Hershenson does not teach or suggest that the target model for a device (i.e., for a component of the integrated circuit) is created using a target performance parameter range for a performance attribute of the device, much less that the target performance parameter range of the device's performance attribute comprises both "multiple first bounded ranges" and "a second bound range".

The Office Action provides that Hershenson teaches "each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point (HE'277:Col. 20 Lines 6-21, Col. 21 Lines 10-60; Also See Col. 20 Lines 27-60; performance point Col. 21 Lines 35-49). The Applicants respectfully disagree.

As discussed above, Hershenson at col. 20, line 6-col. 21, line 67, discusses a method of developing circuit designs that meet a set of specifications for a set of values of parameters. "The basic idea is to list a set of possible parameters, and to replicate design constraints for all possible parameter values" (see col. 20, lines 13-15). Nothing in the cited portion of Hershenson

indicates that each one of multiple first bounded ranges comprises "a range of performance parameter variations due to manufacturing process variations", much less that each one is "based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point."

The Office Action provides that Hershenson teaches "each of the multiple different designs is directed to a variation of a single design for the said integrated circuit, as variation is topology to optimize various parameters (HE '277: Col. 6 Lines 1-24). The second bounded range is constrained by these curves. The Applicants respectfully disagree.

As discussed previously, Hershenson at col. 5, lines 40-63, discloses a CAD library that stores transistor models, including but not limited to posynomial transistor models of different levels of complexity. Then, a user selects a transistor model (e.g., a posynomial transistor model) as needed based on the design requirements and after the transistor model is selected it is processed by the system. Specifically, col. 6, lines 1-24, of Hershenson, discusses the fact that after selecting a transistor model, a circuit topology and circuit performance specifications, the system generates a geometric program for the defined performance specifications. Nothing in the cited portion of Hershenson teaches or discloses that the system uses multiple different designs for the device that are directed to a variation of a single design for the integrated circuit, rather as set out above only a single transistor model is selected and the integrated circuit design is optimized in light of that transistor model selection.

It is unclear what the Examiner is referring to by the statement "The second bounded range is constrained by these curves." Nothing in the cited portion of Hershenson (i.e., col. 6, lines 1-24) teaches or discloses multiple model curves, much less that a second bounded range of

a target performance parameter range of a performance attribute of a device in an integrated circuit is constrained by "at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device."

Therefore, independent claims 1, 9, 14, 19, 24, 36, 40 and 42 are patentable over Hershenson in combination with Krivokapic and/or the Applicants' admissions. Furthermore, dependent claims 2-3, 5-8, 10-11, 13, 15-18, 20-22, 25-35, 37-39 and 41 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

IV. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-3, 5-11, 13-22, and 24-42, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: August 28, 2007

/Pamela M. Riley/
Pamela M. Riley, Esq.
Registration No. 40,146

Gibb & Rahman, LLC
2568-A Riva Road, Suite 304
Annapolis, MD 21401
Voice: (410) 573-0227
Fax: (301) 261-8825
Customer Number: 29154